

Development of a test circuit for calibration of transducers for high voltage power quality measurements using modelling and computer simulation

**HÉDIO TATIZAWA¹, ERASMO SILVEIRA NETO², GERALDO F. BURANI¹,
ANTÔNIO A. C. ARRUDA¹, KLEIBER T. SOLETO¹, NELSONM. MATSUO¹**

² Companhia de Transmissão de Energia Elétrica Paulista - ISA CTEEP

¹ Instituto de Eletrotécnica e Energia da USP - IEE/USP

Av. Prof. Luciano Gualberto, 1289 - São Paulo

BRAZIL

hedio@iee.usp.br <http://www.iee.usp.br>

Abstract: - The control of power quality parameters in the electric grid is becoming much more important, considering the increasing of sensitive loads, and also the consumers' awareness claiming for a better quality of the electrical energy supply [1,2,3,4]. Most of the necessary calibration procedures for power quality monitors and power quality analyzers are already defined in the international standards, mainly in the IEC 61000 series [5] and ANSI/IEEE Standards. This paper presents results of a research intended to develop a methodology for the calibration of high voltage transducers for power quality measurements in high voltage networks, considering that such kind of procedures are not yet established in the pertinent standards. In this research it is also considered that the conventional high voltage laboratory is not suitable for power quality tests, so some improvement is necessary on this subject. In this development, modeling and computer simulation using ATP-Alternative Transients Program [6] were used for to assess the frequency response of the test setup, and the design of the reactive compensation of the test circuit.

Key-Words: - high voltage transducers, capacitive voltage dividers, power quality measurements, harmonics, IEC 61000 series, high voltage.